SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
Accredited by National Board of Accreditation,
AICTE, New Delhi, Accredited by NAAC with "A" Grade – 3.32 CGPA
Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi,
Permanent Affiliation to JNTUK, Kakinada
SEETHARAMPURAM, W.G.DT., NARSAPUR-534280, (Andhra Pradesh)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING PLAN

Course Code	Course Title	Semester	Branch	Contact Period /Week	Academic Year	Semester commencement date
20EC3T06	Digital Logic Design (R20)	III	CSE	5	2021-22	25-10-2021

COURSE OUTCOMES

After completion of the course student are able to

1	Understand the function of digital systems (K1)
2	Analyze Boolean functions with basic theorems and properties.(K4)
3	Explain the behavior of various combinational circuits (K2,K4)
4	Construct digital systems using sequential circuits (K3)

Unit No	OutCome/ Bloom's Level		Topics/Actvity	Reference Text book	Contact Periods	Delivery Method
1	CO1: Understand the function of digital systems (K1)		**DIGITAL SYSTEMS AND BINARY NUMBERS**			Chalk & Talk, PPT, Active Learning & Tutorial
		1.1	Digital Systems, Review of number systems	T1,T2,R1	1	
		1.2	Special codes like Excess-3 codes	T1,T2,R1	1	
		1.3	Excess-3 addition & subtraction	T1,T2,R1	1	
		1.4	Gray codes	T1,T2,R1	1	
		1.5	Complements of Numbers-Unsigned binary numbers	T1,T2,R1	1	
		1.6	Signed Binary Numbers	T1,T2,R1	1	
		1.7	Arithmetic addition and subtraction	T1,T2,R1	1	
		1.8	BCD codes - BCD Addition	T1,T2,R1	1	
		1.9	BCD Subtraction	T1,T2,R1	1	
		1.10	Review of logic gates	T1,T2,R1	1	
		1.11	UNIT TEST-I		1	
			TOTAL		**11**	
			CONCEPT OF BOOLEAN ALGEBRA			
		2.1	Basic Theorems	T1,T2, R2	1	
		2.2	Properties of Boolean algebra	T1,T2, R2	1	
		2.3	Boolean Functions	T1,T2, R2	1	
		2.4	Canonical and Standard Forms,	T1,T2, R2	1	

2.	CO2: Analyze Boolean functions with basic theorems and properties.(K4)		Minterms and Maxterms			Chalk & Talk, PPT, Active Learning & Tutorial
		2.5	Simplification of Boolean expression using Boolean laws	T1,T2, R2	1	
		2.6	Map Method, Three-Variable K-Map	T1,T2, R2	2	
		2.7	Four Variable K-Maps	T1,T2, R2	1	
		2.8	K-maps with don't care conditions	T1,T2, R2	1	
		2.9	Implementation of logic gates using NAND function.	T1,T2, R2	1	
		2.10	Implementation of logic gates using NOR function.	T1,T2, R2	1	
		2.11	UNIT TEST - II		1	
			TOTAL		**12**	

3.	CO3: Explain the behavior of various combinational circuits (K2,K4)		**COMBINATIONAL LOGIC**			Chalk & Talk, PPT, Active Learning & Case study
		3.1	Introduction, Binary Adder- Half & Full Adder	T1,T2,R3	2	
		3.2	Half & Full subtractor	T1,T2, R3	1	
		3.3	Binary Multiplier	T1,T2, R3	1	
		3.4	Decoders	T1,T2, R3	1	
		3.5	Encoders,	T1,T2, R3	1	
		3.6	Multiplexers	T1,T2, R3	1	
		3.7	De multiplexers	T1,T2, R3	1	
		3.8	Priority Encoder	T1,T2, R3	1	
		3.9	Code Converters	T1,T2, R3	1	
		3.10	Magnitude Comparator	T1,T2, R3	2	
		3.11	UNIT TEST - III		1	
			TOTAL		**13**	

4.	CO4:Construct Digital systems using sequential circuits (K3)		**SEQUENTIAL LOGIC – I**			Chalk & Talk,PPT, Active Learning & Project based learning
		4.1	Introduction to Sequential Circuits	T1,T2,R1	1	
		4.2	Storage Elements: Latches, Flip-Flops	T1,T2,R1	1	
		4.3	RS- Latch Using NAND and NOR Gates, Truth Tables.	T1,T2,R1	1	
		4.4	RS Flip Flops, Truth and Excitation Tables	T1,T2,R1	1	
		4.5	JK Flip Flops, Truth and Excitation Tables	T1,T2,R1	1	
		4.6	T Flip Flops, Truth and Excitation Tables	T1,T2,R1	1	
		4.7	D Flip Flops, Truth and Excitation Tables	T1,T2,R1	1	

		4.8	Realization of Switching Functions using PROM,	T1,T2,R1	1	
		4.9	Realization of Switching Functions using PAL	T1,T2,R1	1	
		4.10	Realization of Switching Functions using PLA	T1,T2,R1	1	
		4.11	UNIT TEST - IV		1	
				TOTAL	**11**	
			SEQUENTIAL LOGIC-II			
5.	CO4:Construct Digital systems using combinational and/or sequential circuits (K3)	5.1	Conversion of flip flops	T1,T2,R1	2	Chalk & Talk, PPT, Active Learning & Tutorial
		5.2	Registers, Shift Registers	T1,T2,R1	1	
		5.3	Shift Registers: SISO	T1,T2,R1	1	
		5.4	Shift Registers: SIPO	T1,T2,R1	1	
		5.5	Shift Registers: PISO	T1,T2,R1	1	
		5.6	Shift Registers: PIPO	T1,T2,R1	1	
		5.7	Ripple Counters	T1,T2,R1	1	
		5.8	Design of n-bit Synchronous Counters	T1,T2,R1	1	
		5.9	Up-Down counter	T1,T2,R1	1	
		5.10	Ring Counter	T1,T2,R1	1	
		5.11	Johnson Counter.	T1,T2,R1	1	
		5.12	UNIT TEST - V		1	
				TOTAL	**13**	
	Additional topics		Mealy and Moore machines	T1,R1,R2		
TOTAL NO. OF CLASSES PROPOSED PER PERIOD'S					**60**	

Text Books:	
S.No.	**AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION**
1	M. Morris Mano, "Digital Design", 4th Edition, Prentice Hall of India Pvt. Ltd., 2008 / Pearson Education (Singapore) Pvt. Ltd., New Delhi, 2003.**(Unit I, II, III, IV, V)**
2	Charles H.Roth. "Fundamentals of Logic Design", 6th Edition, Thomson Learning, 2013.

Reference Books:	
S.No.	**AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION**
1	John F. Wakerly, "Digital Design", Fourth Edition, Pearson/PHI, 2008
2	John. M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 2006.
3	Donald P. Leach and Albert Paul Malvino, "Digital Principles and Applications", 6th Edition, TMH, 2006

Web Details	
1	www.nptel.ac.in
2	www.slideshare.net
3	https://youtu.be/Z-Hw3CpPVj0

		Name	Signature with Date
i.	Faculty - I	Ms.E.Suma	
ii.	Faculty - II(for common Course)	Mr.T.Jerry Alexander	
iii.	Course Coordinator	Mrs. G. B. Christina	
iv.	Module Coordinator	Mr. J. E. N. Abhilash	
v.	Programme Coordinator	Dr. B. S. Rao	

Principal

Dr. S. Suresh Kumar